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Nano-design of ultra-efficient reversible block based on quantum-dot cellular automata#

Seyed Sajad AHMADPOUR[1], Nima Jafari NAVIMIPOUR‡[1], Mohammad MOSLEH[2], Senay YALCIN[3]

[1]*Department of Computer Engineering, Faculty of Engineering and Natural Sciences, Kadir Has University, Istanbul 34083, Türkiye*

[2]*Materials and Energy Research Center, Dezful Branch, Islamic Azad University, Dezful 6468118333, Iran*

[3]*Department of Computer Engineering, Nisantasi University, Istanbul 34485, Türkiye*

Email: Seyed.Ahmad@khas.edu.tr; Nima.navimipour@khas.edu.tr; Mosleh@iaud.ac.ir; senay.yalcin@nisantasi.edu.tr

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Abstract: Reversible logic has recently gained significant interest due to its inherent ability to reduce energy dissipation, which is the primary need for low-power digital circuits. One of the newest areas of relevant study is reversible logic, which has applications in many areas, including nanotechnology, DNA computing, quantum computing, fault tolerance, and low-power complementary metal-oxide-semiconductor (CMOS). An electrical circuit is classified as reversible if it has an equal number of inputs and outputs, and a one-to-one relationship. A reversible circuit is conservative if the EXOR of the inputs and the EXOR of the outputs are equivalent. In addition, quantum-dot cellular automata (QCA) is one of the state-of-the-art approaches that can be used as an alternative to traditional technologies. Hence, we propose an efficient conservative gate with low power demand and high speed in this paper. First, we present a reversible gate called ANG (Ahmadpour Navimipour Gate). Then, two non-resistant QCA ANG and reversible fault-tolerant ANG structures are implemented in QCA technology. The suggested reversible gate is realized through the Miller algorithm. Subsequently, reversible fault-tolerant ANG is implemented by the 2DW clocking scheme. Furthermore, the power consumption of the suggested ANG is assessed under different energy ranges (0.5Ek, 1.0Ek, and 1.5Ek). Simulations of the structures and analysis of their power consumption are performed using QCADesigner 2.0.03 and QCAPro software. The proposed gate shows great improvements compared to recent designs.

Key words: Nanotechnology; Reversible logic; Energy dissipation; Quantum-dot cellular automata (QCA); Reversible gate; Miller algorithm

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1 Introduction

Recently, nano-circuits and nano-designs have received much attention in a wide range of domains (Miller et al., 2003). Nanoscale reversible-based designs have been in the research focus as they exhibit reduced heat dissipation (Roohi et al., 2018). Landauer (1961) showed that in a non-reversible computation, the loss of each bit of information produces a $kT\ln 2$ (J) of heat energy, where k stands for Boltzmann's constant and T denotes absolute computing temperature. Furthermore, Bennett (1973) proved that the $kT\ln 2$ (J) energy would not be eliminated when the computation is carried out reversibly (Pramanik et al., 2022). In other words, one of the important rules in reversible circuits that can reduce energy consumption is that the number of inputs is the same as the number of outputs (Bennett, 1973).

On the other hand, the complementary metal-oxide-semiconductor (CMOS) is saturated in terms of power efficiency and feature size (Norouzi et al.,

‡ Corresponding author

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ORCID: Seyed Sajad AHMADPOUR, https://orcid.org/0000-0003-2462-8030; Nima Jafari NAVIMIPOUR, https://orcid.org/0000-0002-5514-5536

2020). In addition, this technology is facing a significant challenge in operating at the nanoscale range because of its physical restrictions, such as short channel effects, doping fluctuations, ultra-thin gate oxides, excess power dissipation, and expensive fabrication process. Recently, the cellular automaton has been applied in a wide range of scenarios (Norouzi et al., 2020). In this regard, quantum-dot cellular automata (QCA) technology has received tremendous attention as a worthwhile substitute for CMOS technology owing to its area efficiency and extremely low power consumption rate (Norouzi et al., 2020; Roy et al., 2021; Safaiezadeh et al., 2022). Furthermore, QCA cells are the primary elements in any QCA circuit (Norouzi et al., 2020; Roy et al., 2021). In QCA, there is no current flow; hence, it only has intercellular interactions through Coulombic repulsion. The fundamental gates in QCA technology have been developed based on two important structures, i.e., three-input majority voters (MV3) and inverters (INVs), which are used to synthesize any complex QCA logic circuit. Unlike CMOS, in QCA, primitive Boolean logic (AND/OR) cannot be generated directly; instead, MV3 is used to produce such primitive Boolean logic.

This paper first presents an efficient reversible gate called ANG (Ahmadpour Navimipour Gate). ANG is proved using the Miller algorithm. In addition, two non-resistant QCA ANG and fault-tolerant QCA ANG structures are implemented using the ANG in QCA technology. The non-resistant QCA ANG is verified through physical evidence. Moreover, ANG is measured in terms of cost and 13 standard functions. The results indicate that the suggested gate is more efficient than the previous structures regarding power dissipation, delay, and complexity.

2 Related works

A conservative block performs important functions in digital systems due to its wide application in reversible logic. In this section, we introduce the six most important gates, including double Feynman gate (DFG) (Parhami, 2006), Fredkin gate (FRG) (Fredkin and Toffoli, 1982), new fault tolerance gate (NFT) (Haghparast and Navi, 2008a), proposed parity reversible gate (PPRG) (Roohi et al., 2018), proposed Norallahzadeh Mosleh1 (PNM1), and proposed Norallahzadeh Mosleh2 (PNM2) (Noorallahzadeh and Mosleh, 2020), which are shown in Figs. S1–S6 in the supplementary materials.

DFG: The truth table of the 3×3 parity preserving reversible DFG is shown in Table S1. It has three-input vectors $\boldsymbol{I}_{\mathrm{V}}$ ($\boldsymbol{A}$, $\boldsymbol{B}$, and $\boldsymbol{C}$) and three-output vectors $\boldsymbol{O}_{\mathrm{V}}$ ($\boldsymbol{P}$, $\boldsymbol{Q}$, and $\boldsymbol{R}$). The output is given by $\boldsymbol{P}=\boldsymbol{A}$, $\boldsymbol{Q}=\boldsymbol{A}\oplus\boldsymbol{B}$, and $\boldsymbol{R}=\boldsymbol{A}\oplus\boldsymbol{C}$. Its logical calculation is 2α.

FRG: The truth table of the 3×3 parity preserving reversible FRG is shown in Table S2. It has three-input vectors $\boldsymbol{I}_{\mathrm{V}}$ ($\boldsymbol{A}$, $\boldsymbol{B}$, and $\boldsymbol{C}$) and three-output vectors $\boldsymbol{O}_{\mathrm{V}}$ ($\boldsymbol{P}$, $\boldsymbol{Q}$, and $\boldsymbol{R}$). The output is given by $\boldsymbol{P}=\boldsymbol{A}$, $\boldsymbol{Q}=\boldsymbol{A'B}\oplus\boldsymbol{AC}$, and $\boldsymbol{R}=\boldsymbol{A'C}\oplus\boldsymbol{AB}$. Its logical calculation is $2\alpha+4\beta+2\delta$.

NFT: The truth table of the 3×3 parity preserving reversible NFT is shown in Table S3. It has three-input vectors $\boldsymbol{I}_{\mathrm{V}}$ ($\boldsymbol{A}$, $\boldsymbol{B}$, and $\boldsymbol{C}$) and three-output vectors $\boldsymbol{O}_{\mathrm{V}}$ ($\boldsymbol{P}$, $\boldsymbol{Q}$, and $\boldsymbol{R}$). The output is given by $\boldsymbol{P}=\boldsymbol{A}\oplus\boldsymbol{B}$, $\boldsymbol{Q}=\boldsymbol{B'C}\oplus\boldsymbol{AC'}$, and $\boldsymbol{R}=\boldsymbol{BC}\oplus\boldsymbol{AC'}$. Its logical calculation is $3\alpha+4\beta+3\delta$.

PPRG: The truth table of the 3×3 parity preserving PPRG is shown in Table S4. It has three-input vectors $\boldsymbol{I}_{\mathrm{V}}$ ($\boldsymbol{A}$, $\boldsymbol{B}$, and $\boldsymbol{C}$) and three-output vectors $\boldsymbol{O}_{\mathrm{V}}$ ($\boldsymbol{P}$, $\boldsymbol{Q}$, and $\boldsymbol{R}$). The output is given by $\boldsymbol{P}=\boldsymbol{A}\oplus\boldsymbol{B}$, $\boldsymbol{Q}=\boldsymbol{AC}\oplus\boldsymbol{B'C'}$, and $\boldsymbol{R}=\boldsymbol{A'C}\oplus\boldsymbol{B'C'}$. Its logical calculation is $3\alpha+4\beta+3\delta$.

PNM1: The truth table of the 4×4 parity preserving PNM1 is shown in Table S5. It has four-input vectors $\boldsymbol{I}_{\mathrm{V}}$ ($\boldsymbol{A}$, $\boldsymbol{B}$, $\boldsymbol{C}$, and $\boldsymbol{D}$) and four-output vectors $\boldsymbol{O}_{\mathrm{V}}$ ($\boldsymbol{P}$, $\boldsymbol{Q}$, $\boldsymbol{R}$, and $\boldsymbol{S}$). The output is given by $\boldsymbol{P}=(\boldsymbol{A}\oplus\boldsymbol{B})'$, $\boldsymbol{Q}=\boldsymbol{B'}$, $\boldsymbol{R}=\boldsymbol{B'C}\oplus\boldsymbol{BD}$, and $\boldsymbol{S}=\boldsymbol{B'D}\oplus\boldsymbol{BC'}$. Its logical calculation is $4\alpha+8\beta+4\delta$.

PNM2: The truth table of the 4×4 parity preserving PNM2 is shown in Table S6. It has four-input vectors $\boldsymbol{I}_{\mathrm{V}}$ ($\boldsymbol{A}$, $\boldsymbol{B}$, $\boldsymbol{C}$, and $\boldsymbol{D}$) and four-output vectors $\boldsymbol{O}_{\mathrm{V}}$ ($\boldsymbol{P}$, $\boldsymbol{Q}$, $\boldsymbol{R}$, and $\boldsymbol{S}$). The output is given by $\boldsymbol{P}=\boldsymbol{AC'}\oplus\boldsymbol{BC}$, $\boldsymbol{Q}=(\boldsymbol{A}\oplus\boldsymbol{B})'$, $\boldsymbol{R}=\boldsymbol{C'}$, and $\boldsymbol{S}=\boldsymbol{AC'}\oplus\boldsymbol{BC}\oplus\boldsymbol{D}$. Its logical calculation is $4\alpha+8\beta+4\delta$.

3 Suggested reversible design

3.1 Proofing proposed ANG using Miller's algorithm

This section presents the suggested reversible gate using Miller's algorithm (Miller et al., 2003). Finally, two QCA structures are developed based on ANG. All outputs can be achieved according to Eqs. (1)–(3):

$$\boldsymbol{P} = \boldsymbol{BC} + \boldsymbol{A}\bar{\boldsymbol{B}}, \quad (1)$$

$$\boldsymbol{Q} = \boldsymbol{B}\bar{\boldsymbol{C}} + \boldsymbol{AC}, \quad (2)$$

$$\boldsymbol{R} = \bar{\boldsymbol{A}}\boldsymbol{C} + \boldsymbol{AB}. \quad (3)$$

The circuit view and quantum realization of the suggested reversible block are presented in Fig. 1.

To estimate the quantum cost of the ANG, it must be constructed using the algorithm proposed by Miller et al. (2003). Table 1 shows the steps to be followed by Miller's algorithm to obtain the suggested block.

An $n\times n$ Toffoli gate (TFn(x_1, x_2, $\cdots$, x_n)) contains $n-1$ control inputs that are transmitted via the gate and kept unchanged plus a target input on which the value is inverted, provided that all the control inputs have values equal to "1." In addition, TF1($\boldsymbol{A}$) represents a special case with no control lines.

The steps taken to implement the Miller synthesis (Table 1) are as follows:

Stage 1: Identify TF2($\boldsymbol{P}$, $\boldsymbol{Q}$);

Stage 2: Identify TF3($\boldsymbol{R}$, $\boldsymbol{Q}$, $\boldsymbol{P}$);

Stage 3: Identify TF2($\boldsymbol{P}$, $\boldsymbol{Q}$);

Stage 4: Identify TF3($\boldsymbol{P}$, $\boldsymbol{Q}$, $\boldsymbol{R}$);

Stage 5: Identify TF3($\boldsymbol{P}$, $\boldsymbol{R}$, $\boldsymbol{Q}$);

Stage 6: Identify TF3($\boldsymbol{P}$, $\boldsymbol{Q}$, $\boldsymbol{R}$).

Fig. 2 demonstrates the circuit using Toffoli of the ANG.

Since the quantum cost of the basic gates 1×1 and 2×2 is equal to one, the non-optimal quantum cost of ANG equals 14. Fig. 3 displays the NOT-controlled V (NCV) representation of the suggested ANG.

The quantum circuit illustrated in Fig. 3 is simplified using the reduction rules. In addition, the optimized NCV display of the ANG is demonstrated in Fig. 4. Eventually, the quantum cost of the ANG is equal to 10.

3.2 Implementation of the reversible ANG in QCA technology

The recommended reversible gate in QCA technology is put into practice in this part. In addition,

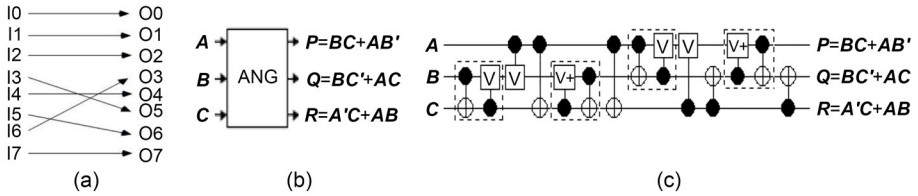

Fig. 1 The suggested reversible block: (a) input-output ratio of the ANG block; (b) circuit view; (c) quantum realization

Table 1 Steps applied to the Miller synthesis on the ANG block

Input			Output			1			2			3			4			5			6		
A	***B***	***C***	***P***	***Q***	***R***	***P***	***Q***	***R***	***P***	***Q***	***R***	***P***	***Q***	***R***	***P***	***Q***	***R***	***P***	***Q***	***R***	***P***	***Q***	***R***
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
0	**0**	**1**	**0**	**0**	**1**	**0**	**0**	**1**	**0**	**0**	**1**	**0**	**0**	**1**	**0**	**0**	**1**	**0**	**0**	**1**	**0**	**0**	**1**
0	**1**	**0**	**0**	**1**	**0**	**0**	**1**	**0**	**0**	**1**	**0**	**0**	**1**	**0**	**0**	**1**	**0**	**0**	**1**	**0**	**0**	**1**	**0**
0	**1**	**1**	**1**	**0**	**1**	**1**	**1**	**1**	**0**	**1**	**1**	**0**	**1**	**1**	**0**	**1**	**1**	**0**	**1**	**1**	**0**	**1**	**1**
1	**0**	**0**	**1**	**0**	**0**	**1**	**1**	**0**	**1**	**1**	**0**	**1**	**0**	**0**	**1**	**0**	**0**	**1**	**0**	**0**	**1**	**0**	**0**
1	**0**	**1**	**1**	**1**	**0**	**1**	**0**	**0**	**1**	**0**	**0**	**1**	**1**	**0**	**1**	**1**	**1**	**1**	**0**	**1**	**1**	**0**	**1**
1	**1**	**0**	**0**	**1**	**1**	**0**	**1**	**1**	**1**	**1**	**1**	**1**	**0**	**1**	**1**	**0**	**1**	**1**	**1**	**1**	**1**	**1**	**0**
1	**1**	**1**	**1**	**1**	**1**	**1**	**0**	**1**	**1**	**0**	**1**	**1**	**1**	**1**	**1**	**1**	**0**	**1**	**1**	**0**	**1**	**1**	**1**

1: if $\boldsymbol{P}$=**1** then invert $\boldsymbol{Q}$; 2: if $\boldsymbol{R}$=$\boldsymbol{Q}$=**1** then invert $\boldsymbol{P}$; 3: if $\boldsymbol{P}$=**1** then invert $\boldsymbol{Q}$; 4: if $\boldsymbol{P}$=$\boldsymbol{Q}$=**1** then invert $\boldsymbol{R}$; 5: if $\boldsymbol{P}$=$\boldsymbol{R}$=**1** then invert $\boldsymbol{Q}$; 6: if $\boldsymbol{P}$=$\boldsymbol{Q}$=**1** then invert $\boldsymbol{R}$

Fig. 2 NOT-CNOT-Toffoli (NCT) based circuit of the proposed ANG

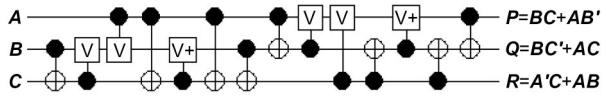

Fig. 3 NCV-based circuit of the proposed ANG

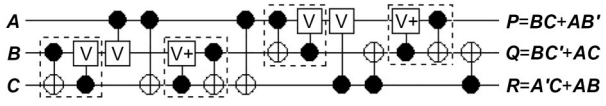

Fig. 4 Optimized NCV of the ANG

the gate functionality is to be evaluated by physical evidence and power consumption analysis. All simulations are performed using the QCADesigner 2.0.3 simulator with default parameter values (Walus et al., 2004). The suggested reversible gate is made in the form of two non-resistant QCA ANG and fault-tolerant QCA ANG structures. The non-resistant QCA ANG and fault-tolerant QCA ANG structures are developed using the non-resistant majority (Walus et al., 2004) and resistant gates (Ahmadpour and Mosleh, 2020). The proposed non-resistant QCA ANG consists of 165 cells, has an area of 0.18 μm^2, and its output equals 6 clock cycles (latency).

The proposed non-resistant QCA ANG is significantly better than PPRG (Roohi et al., 2018) and PNM (Noorallahzadeh and Mosleh, 2020) in cell count, area, and latency. In addition, the cell count and area of the suggested non-resistant QCA ANG structure achieve 3.5% and 5.26% improvements respectively, compared to those of PPRG (Roohi et al., 2018) design. Moreover, the cell count, area, and latency of the suggested non-resistant QCA ANG structure show 24.19%, 56.74%, and 48.52% improvements respectively, compared to those of the previous optimal PNM (Noorallahzadeh and Mosleh, 2020). Besides, all inputs of the PPRG (Roohi et al., 2018) design were mixed together. It is not easy to develop highly efficient designs such as content-addressable memory (CAM) address, shift register, and divider. In the PNM (Noorallahzadeh and Mosleh, 2020), inputs and outputs are in a closed loop; therefore, it is not possible to design and implement complex circuits such as adder (Ahmadpour et al., 2022), multiplier (Bahar and Wahid, 2020), divider, and CPU, based on the PNM. Meanwhile, none of the inputs and outputs of the suggested non-resistant QCA ANG structure are in a closed loop, so that it can provide a valuable basis for all quantum researchers to design and develop their proposed design. The cellular structure and output of the suggested gate are demonstrated in Fig. 5.

As depicted in Fig. 5, following Abedi et al. (2015), we used a non-resistant QCA ANG approach with different clock areas in our scheme. The proposed fault-tolerant QCA ANG structure includes 339 cells, has an area of 0.39 μm^2, and its output is equal to 5 clock cycles (latency).

The proposed fault-tolerant QCA ANG is more tolerant than PPRG (Roohi et al., 2018) and PNM (Noorallahzadeh and Mosleh, 2020) in single-cell defects and misalignments defects. It achieves 80.58% and 69.41% improvement compared to PPRG, respectively, and 75.35% and 55.09% improvement compared to the previous optimal PNM, respectively. Furthermore, not all quantum cells of the PPRG and optimal PNM designs are resistant, so they are not suitable for an unstable situation. Meanwhile, the proposed fault-tolerant QCA ANG is better than PNM in terms of cell count and area, and achieves 12.34% and 7.87% improvement compared to the PPRG design, respectively. The cellular structure and output of the proposed ANG are shown in Fig. 6.

In these two gates, the inputs and outputs are not in a closed loop and can be easily accessed. All complex structures can be proposed based on these two gates because the inputs and outputs are not mixed. Moreover, the best coplanar layout has been used to propose these two gates, and this will make them single-layer because multilayer circuits have less stability and higher energy consumption. Finally, the outputs of both gates have very high polarity and can easily be used to connect to larger circuits such as mux, adder, and arithmetic logic unit (ALU).

The suggested ANG block is validated using the physical proofs in the following section.

3.3 Physical proofs

Eq. (4) is used to calculate the energy between two electrons:

$$U = \frac{kq_iq_j}{r}\ (\mathrm{J}), \tag{4}$$

where U denotes the kink energy, k is Coulomb's constant, q_i and q_j denote electron charges, and r is the distance between essential electron charges. Finally, U is calculated based on Joule energy using Eq. (5):

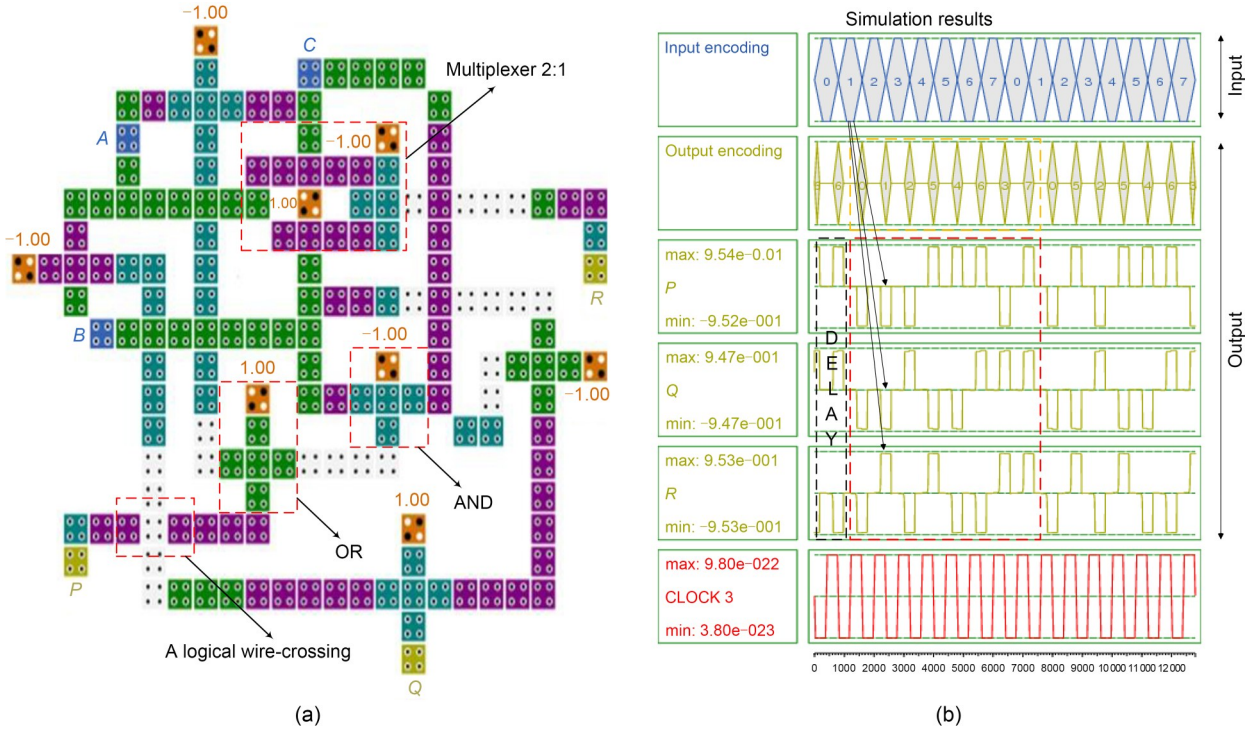

Fig. 5 Suggested non-resistant QCA ANG: (a) cellular structure; (b) outputs

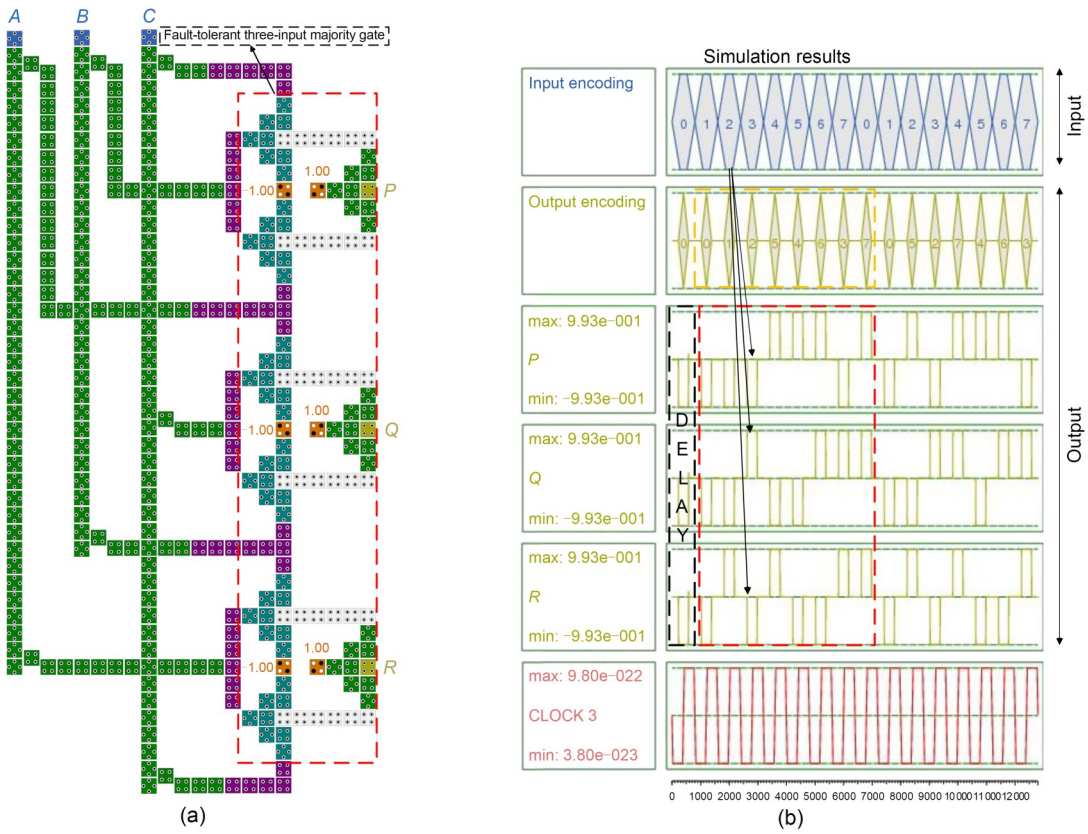

Fig. 6 The proposed fault-tolerant QCA ANG: (a) cellular structure; (b) outputs

$$U = \frac{9 \times 10^{9} \times 1.6^{2} \times 10^{-38}}{r} = \frac{23.04 \times 10^{-29}}{r}. \quad (5)$$

Since measuring the outputs is a highly demanding task involving many computations, we decide to compute merely the outputs for the optional vectors (***A***=**0**, ***B***=**1**, and ***C***=**0**). This technique can be simply applied to each input. Fig. 7 illustrates the electron positions of all suggested ANG quantum cells. The cellular network affecting cells (e_1 to e_8) using a couple of polarities of "+1" and "−1" is presented in Figs. 8a and 8b. The kink energies are applied to each electron, e_1 to e_8, along with electrons x and y, as seen in these figures.

The polarity of cell ***P*** has the value of "1," which confirms the suggested cellular structure.

3.4 QCA clocking

All structures require appropriate clocking and synchronization to control information throughout the circuit (Wang Z et al., 2022). In QCA, clocking provides energy to the cells. However, several different cloning schemes have been proposed (Bhanja and Sarkar, 2008; Taskin and Hong, 2008; Vankamamidi et al., 2008; Abedi et al., 2015; Campos et al., 2016). The 2DW (two-dimensional schemes) clocking technique that reduces the length of lines in each time zone was inspired by systolic arrays (Vankamamidi et al., 2008). In this subsection, we discuss the implementation of the suggested reversible fault-tolerant QCA ANG by 2DW clocking, as demonstrated in Fig. S7 in the supplementary materials.

As seen in Fig. S7, the recommended reversible ANG includes 937 cells, with an occupied area of 1.27 μm^2, and its output is generated after 15 clock cycles (latency).

3.5 Power consumption analysis of the proposed ANG

The study of energy and power consumption is critical in almost all designs (Liu et al., 2021; Gong et al., 2022). The power consumption analysis of the suggested ANG was carried out using QCAPro. Table 2

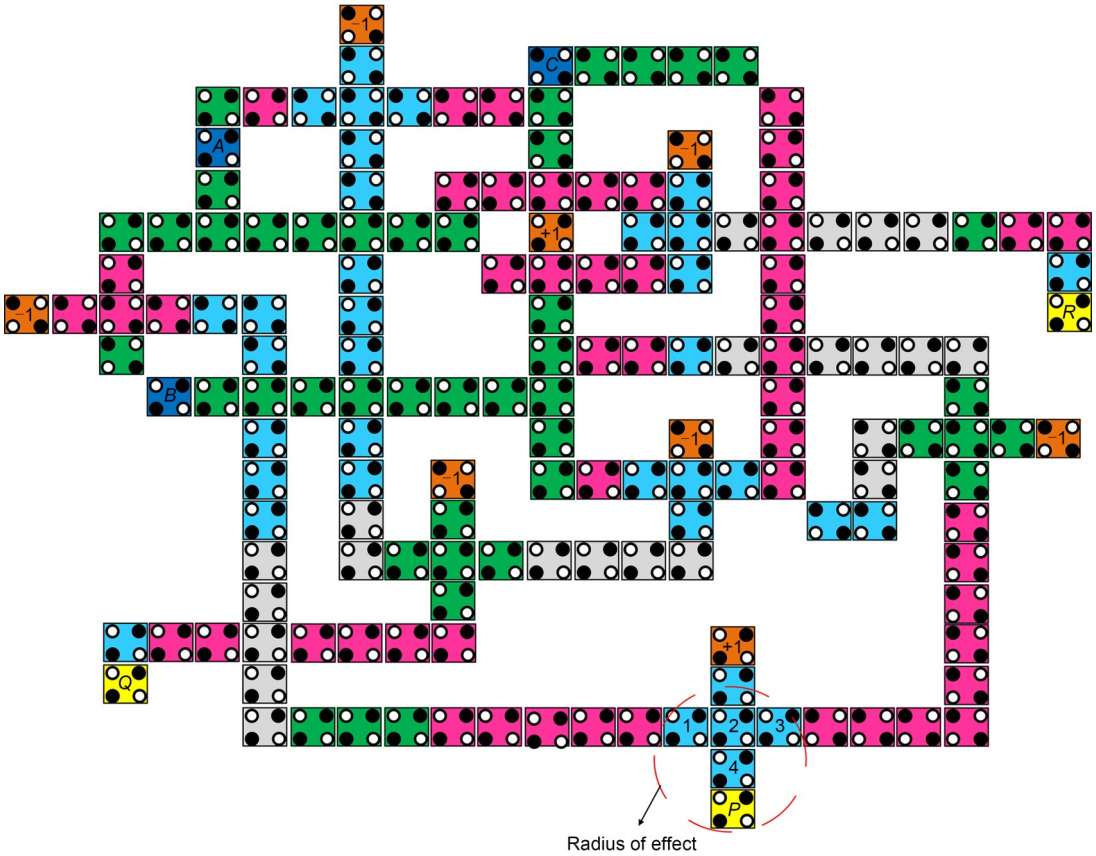

Fig. 7 Cell polarities in the suggested non-resistant QCA ANG

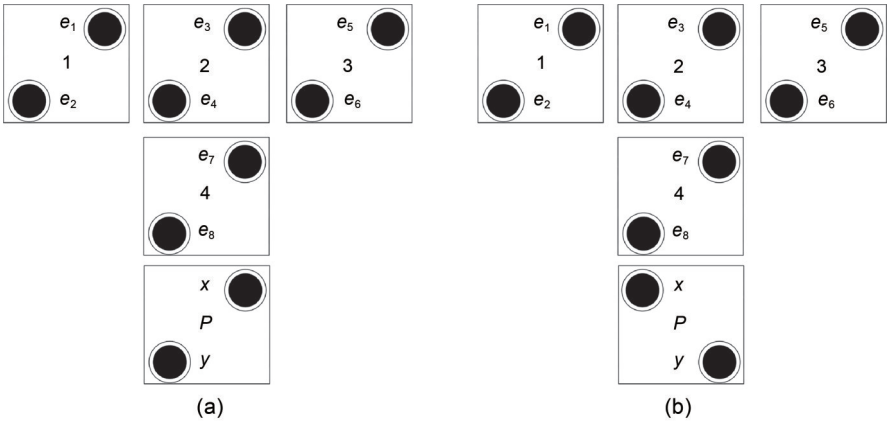

Fig. 8 The cellular network affecting five cells by the polarities of "1" (a) and "0" (b)

Table 2 Power consumption analysis of reversible gates

Design	Average leakage energy dissipation (eV)			Average switching energy dissipation (eV)			Total energy dissipation (eV)		
	0.5Ek	1.0Ek	1.5Ek	0.5Ek	1.0Ek	1.5Ek	0.5Ek	1.0Ek	1.5Ek
DFG (Feynman, 1986)	270.58	758.27	1001.41	658.25	518.67	491.01	928.83	1276.94	1492.42
FRG (Fredkin and Toffoli, 1982)	101.53	283.69	482.40	213.78	175.64	143.28	315.31	459.33	625.68
NFT (Haghparast and Navi, 2008a)	60.58	178.31	299.54	154.35	125.36	107.94	214.93	303.67	407.48
PPRG (Roohi et al., 2018)	58.04	168.07	294.34	193.07	166.15	141.80	251.11	334.22	436.14
PNM1 (Noorallahzadeh and Mosleh, 2020)	100.25	301.57	599.35	611.71	519.69	421.15	711.96	821.26	1020.50
PNM2 (Noorallahzadeh and Mosleh, 2020)	105.46	333.26	606.10	624.61	538.28	453.59	730.07	871.54	1059.38
NMG4 (Noorallahzadeh and Mosleh, 2019)	59.44	171.07	274.34	198.77	167.85	162.90	258.21	338.92	437.24
SCV (Kundu et al., 2022)	56.05	166.41	279.27	168.01	124.70	110.45	224.06	291.11	389.72
Non-resistant QCA ANG	58.78	168.81	268.52	147.14	114.39	104.24	205.92	283.20	372.76
Fault-tolerant QCA ANG	199.49	341.97	516.34	364.81	295.13	242.30	564.30	637.10	758.64

shows the results of the power consumption analysis for the two suggested reversible gates compared with recent blocks.

As shown in Table 2, the two suggested structures are superior to the most recent designs in terms of energy consumption. The suggested non-resistant QCA ANG is better than all recent structures in power consumption at three levels of 0.5Ek, 1.0Ek, and 1.5Ek. Its total energy consumption achieves 4.19%, 6.74%, and 8.52% improvement, corresponding to three levels of 0.5Ek, 1.0Ek, and 1.5Ek, respectively, compared to the previous NFT design (Haghparast and Navi, 2008a). Besides, the proposed fault-tolerant QCA ANG structure is superior to most recent methods in this regard.

3.6 Cost of QCA-based circuits

The cost of QCA-based circuits is a vital parameter for evaluating QCA structures, and is calculated as Cost QCA=$(M^2+I+C^2)T$, where M, I, and C stand for the numbers of MVs, INVs, and crossings, respectively, and T represents the delay. Table 3 lists the numbers of QCA-reversible MVs, INVs, crossings, and delay for each type of gate. Notably, delay controlling plays a vital role in measuring the success of the designs in a wide range of applications (Wang JW et al., 2022). The complexity of the QCA-reversible gate is given as $M+I+C$. The table contains data to compare the two proposed ANG structures with the previous blocks.

As shown in Table 3, the two proposed structures are superior to most of earlier designs in terms of the cost function. The suggested non-resistant QCA ANG cost is higher than those of previous designs except the designs introduced in two references (Haghparast and Navi, 2008b; Noorallahzadeh and Mosleh, 2020). The cost of the suggested fault-tolerant QCA ANG is higher than those of previous designs except the designs proposed in three studies (Feynman, 1986;

Haghparast and Navi, 2008b; Noorallahzadeh and Mosleh, 2020). Moreover, the cost of the proposed fault-tolerant QCA ANG structure shows 6.62% improvement over the cost required for DFG.

We assess the proposed block through 13 standard Boolean functions. It is possible to convert all three input Boolean functions to 13 standard functions. In other words, these standard functions cover all 256 Boolean functions for the logical synthesis of the three variables. Table 4 shows the 13 standard functions for the proposed block and the previous gates. It can be seen that the suggested reversible block is superior to all recent designs except for NFT and PPRG.

4 Conclusions and suggestions for future research

We first presented a conservative reversible gate called ANG. Then, the gate was used to develop two non-resistant and fault-tolerant QCA layout structures implemented in QCA technology. Fault-tolerant QCA

Table 3 Cost comparison of the QCA-reversible blocks

Design	M	I	T^*	C	Cost function
DFG (Feynman, 1986)	8n	3n	1.50 (6)	4n	498
FRG (Fredkin and Toffoli, 1982)	6n	2n	1.50 (6)	5n	378
NFT (Haghparast and Navi, 2008b)	8n	5n	1.25 (8)	4n	680
PPRG (Roohi et al., 2018)	6n	6n	1.25 (5)	3n	255
PNM1 (Noorallahzadeh and Mosleh, 2020)	7n	3n	2.75 (11)	6n	968
PNM2 (Noorallahzadeh and Mosleh, 2020)	6n	2n	2.50 (10)	6n	740
Non-resistant QCA ANG	9n	3n	1.75 (7)	3n	651
Fault-tolerant QCA ANG	9n	3n	1.25 (5)	3n	465

M, I, and C represent the numbers of majority voters, inverters, and crossings, respectively, and T represents the delay. * The number in the brackets represents the number of clock cycles

Table 4 Standard functions realization for reversible blocks

Function	DFG	FRG	NFT	PPRG	PNM1	PNM2	Proposed
Parity preserving	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Bit conservative	No	Yes	No	No	No	No	Yes
$F = ABC$	2	2	2	2	2	2	2
$F = AB$	1	1	1	1	1	1	1
$F = ABC + A\overline{BC}$	2	3	2	2	3	2	2
$F = ABC + \overline{ABC}$	8	4	3	3	6	7	6
$F = AB + BC$	2	2	2	2	2	2	2
$F = BC + \overline{ABC}$	6	5	3	2	5	5	3
$F = ABC + \overline{A}\,B\,\overline{C} + A\overline{BC}$	6	6	3	3	6	5	5
$F=A$	1	1	1	1	1	1	1
$F = AB + BC + CA$	1	5	4	5	1	1	3
$F = AB + \overline{B}\,C$	4	1	1	1	3	4	3
$F = AB + BC + \overline{ABC}$	2	6	3	2	6	6	4
$F = AB + \overline{AB}$	1	2	1	2	4	1	2
$F = ABC + \overline{AB}\,C + A\overline{BC} + \overline{A}\,B\,\overline{C}$	2	3	1	2	3	1	1
Total	38	41	27	28	43	38	35
Improvement (%)	7.89	14.63	−22.85	−20	18.60	7.89	–

Double Feynman gate (DFG): Feynman, 1986; Fredkin gate (FRG): Fredkin and Toffoli, 1982; new fault tolerance gate (NFT): Haghparast and Navi, 2008b; proposed parity reversible gate (PPRG): Roohi et al., 2018; proposed Norallahzadeh Mosleh1 (PNM1): Noorallahzadeh and Mosleh, 2020; proposed Norallahzadeh Mosleh2 (PNM2): Noorallahzadeh and Mosleh, 2020

was implemented based on popular clocking 2DW. In addition, the proposed reversible ANG was validated through the Miller algorithm. The simulations of circuits and their power consumption analysis were performed using QCADesigner 2.0.03 and QCAPro tools, respectively, and the power consumption of the suggested reversible ANG showed 4.19%, 6.74%, and 8.52% improvement over the NFT design corresponding to three levels of 0.5Ek, 1.0Ek, and 1.5Ek, respectively. All three input Boolean functions to 13 standard functions of the proposed block showed that the suggested reversible block was superior to recent designs. The proposed circuits with an outstanding achievement in computing can be used as a building block in designing more complex and efficient structures such as ALU and CPU in future work.

Contributors

Seyed Sajad AHMADPOUR and Nima Jafari NAVIMIPOUR designed the research. Seyed Sajad AHMADPOUR and Senay YALCIN processed the data. Seyed Sajad AHMADPOUR, Nima Jafari NAVIMIPOUR, and Senay YALCIN drafted the paper. All the authors revised and finalized the paper.

Compliance with ethics guidelines

Seyed Sajad AHMADPOUR, Nima Jafari NAVIMIPOUR, Mohammad MOSLEH, and Senay YALCIN declare that they have no conflict of interest.

Data availability

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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List of supplementary materials

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